TECHNICAL DATA

LeCroy

CAMAC Model 2372

Memory Lookup Unit

- **For trigger processors and complex triggers**
- **Arbitrary user defined transfer function**
- **High capacity/speed**
- **Transparent or strobed mode**
- **64 K-bit dual-ported RAM**
- **Access time 60 nsec**
- **Battery backup—2 year integrity**
- **16-bit front panel Data-in, Data-out connectors**

The Model 2372 is a 64 K-bit dual-ported random access memory based upon the Fermilab module ECL-2. Its access time is ≤ 60 nsec. Packaged in a single-width CAMAC module, the unit offers an exceptionally high capacity/speed product while dissipating < 12.W. Battery backup maintains the integrity of the data within the 2372 (for 2 years) when the CAMAC crate is shut off. This continuous memory feature is particularly useful during the startup phases of an experiment. The MLU serves as a fundamental element of a trigger processor. It also may be used to provide complex functions required of trigger logic.

In normal use, the MLU is first downloaded with the required trigger data and then verified via CAMAC. This information, which defines the function of the MLU, is accessed via the front panel for real time applications. The Model 2372 offers 16-bit front panel Data-In and Data-Out connectors, although not all 32 bits may be used at once. The dimensionality of the Model 2372 is selected via CAMAC to serve the application. The dimensionality options are:

DIMENSIONALITY	INPUT WORD SIZE	MEMORY SIZE (WORDS)	OUTPUT WORD SIZE
0	16	64 K	1
1	15	32 K	2
2	14	16 K	4
3	13	8 K	8
4	12	4 K	16

The function of the MLU may be user defined to meet the application. The required function is downloaded via CAMAC. Virtually any function may be defined: angle logic or clusterized track multiplicity are examples of complex trigger functions. When used as a trigger processor element, the MLU may be used for any operation which is a one-to-one mapping. In conjunction with an ADC, the MLU can be loaded with the calibration to energy. The MLU can also be loaded with a digital comparator function or any arith metic calculation, e.g. $E_1 + E_2$, E/c SinΘ, $(X^2 + Y^2)$.

The strobe facilities of the Model 2372 are used in the software selectable Strobed Mode. In this mode, the MLU is strobed by the ECL Input Enable signals, coming from previous logic unit(s). After 60 nsec, the output "word" of the MLU becomes valid along with four ECL Output Ready signals which may be used to strobe the output word into other modules like the 2372. The output word remains static until another Input Enable is received. This automatically accounts for the propagation delay of the unit. Four Output Ready's are supplied to allow the 2372 to drive multiple logic units. Four Input Enables are provided with an Enable condition being defined as their coincidence (unused inputs are set to logical 1).

The Model 2372 may also be used without regard to the strobe logic. In the Transparent Mode, the output of the Model 2372 may change without regard for the Input Enables. This mode bypasses the latch circuitry and thus provides a slight speed advantage, offering a throughput time of only 55 nsec. This difference is reflected in the Input Enable, Output Ready timing when the Transparent Mode is selected.

October 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 2372
MEMORY LOOKUP UNIT

INPUTS

Input Word: Up to 16 bits, ECL levels via 17-pair header. Pin-outs match ECLine Standard. Impedance 100 Ω ± 5%, high impedance by simple user modification. Minimum width 10 nsec in the Strobed mode or 65 nsec in the Transparent mode. Number of active bits depends upon Dimensionality.

Input Enable: Four differential ECL inputs via 2-pin headers. Required only in Strobed mode. Must arrive ≥ 2 nsec after Input word is settled. Minimum width—Strobed mode: 10 nsec, Transparent mode: 65 nsec (if used).

OUTPUTS

Output Word: Up to 16 bits, ECL levels via 17-pair header. Pin-outs match the ECLine Standard. Output width depends upon Operating mode. Number of active bits depends upon Dimensionality.

Output Ready: Four differential ECL outputs via 2-pin headers. Occurs ≥ 5 nsec after the outputs are settled.

Propagation Delay: 60 nsec. Input Enable to Output Ready—Strobed mode. Transparent mode: 20 nsec after a new Input word becomes valid, the Output word becomes indeterminate. The correct Output word appears within 55 nsec of the new Input word.

CONTROL

Dimensionality Control: CAMAC selected via CAMAC Control Register (CCR). Defines the number of inputs and outputs.

Mode Control: CAMAC selected via CCR.
Strobed Mode—The leading Edge of Enable condition (and of four Input Enables, unused inputs set to logical 1 state) latches Input word. Output Ready's become false within 30 nsec. Output word becomes invalid within 30 nsec. New Output word settled and Output Ready's true within ≤ 60 nsec. Ready and Output word remain until the next Enable condition.
Transparent Mode—operates without regard to Input Enables. Output word present for duration of input word after approximately ≤ 55 nsec delay.
Inhibit Mode—disables front panel inputs to allow CAMAC programming of memory.

MEMORY PROTECTION

Continuous Memory: Memory battery back-up. This feature preserves contents of memory and CCR during CAMAC power down. Life of the battery is two years of operation.

CAMAC COMMANDS

F(0)•A(0): Read 1 to 16-bit Output word addressed by CAMAC Address Register (CAR). Increment CAR. Requires operation in Inhibit mode. Inactive bits are not masked and are arbitrary.

F(0)•A(1): Read 16-bit CAR address. Requires operation in Inhibit mode. Inactive bits are set to 1 if F(16)•A(1) was executed after power up.

F(0)•A(2): Read 5-bit CCR word.

F(0)•A(3): Read 1 to 16-bit Output word addressed by front panel Input word. Inactive bits are not masked and are arbitrary.

F(0)•A(4): Read 12 to 16-bit front panel Input Word.

F(16)•A(0): Write 16-bit word into memory location addressed by CAR. Requires operation in Inhibit mode. Write commands are performed with dimensionality of four. See Owner's Manual.

F(16)•A(1): Write 12 to 16-bit CAR address. Dataword at ECL output will change accordingly. Requires operation in Inhibit mode.

F(16)•A(2): Write 5-bit CCR word.

Q: A Q = 1 response is generated for F(16)•A(0) and F(0)•A(0), A Q = 0 response is generated for these commands when CAR reaches terminal count. This Q Response is valid only when CAR has been loaded via F(16)•A(1) after power up.

X: An X = 1 response is generated for any valid N•F•A.